

# **Analyzing Google Workload Traces in gem5**

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## **Motivation**

Warehouse scale computing (WSC) workloads

Google traces released recently for workloads like WebSearch, Ads, Fleet-Wide, Knowledge Graph [1,2]

WSC workloads have special characteristics different from traditional workloads

Simulating these traces can provide quick DSE for WSC architectures



**Goal: Enable simulation of Google** Workload Traces in gem5 and explore their behavior.

Want to try?

Visit: https://github.com/darchr/gem5/tree/gtraces-gem5



Components involved:

**Trace Reader** Traces in **drmemtrace** format

Trace Reader relies on timestamp information to pick a thread. Trace feeds only **memory instructions** to trace players (configurable).



Separate files for each software thread

Trace Player Configurable **max\_ipc** and max\_outstanding\_mem reqs. gem5 can simulate these traces at 1 million instructions per host second.

gem5's cache and memory sub-system

**Overview of Google Trace Player in gem5** 

#### delta charlie 30 30 (GB/s) BW (GB/s) ddr4 ddr4 20 · 20 ddr5 ddr5 hbm2 hbm2 10 10 BW 0 ( 32 32 16 16 Number of trace players Number of trace players whiskey merced 30 30 (GB/s) (GB/s) ddr4 ddr4 20 -20 ddr5 ddr5 hbm2 hbm2 $10 \cdot$ 10 BW BW 0 32 32 16 16 8 8 Number of trace players Number of trace players

How much these traces stress memory systems?

How does the change in the number of trace players impact the observed bandwidth?

#### Configuration

Feature	Value
Cores	8
Core width	8
Frequency	5GHz
Private L1 I\$	32KB
DRAM	HBM, DDR4/5

## How do these traces compare with other HPC Benchmarks?

We compare cache miss rates of different benchmarks.

#### Configuration

Feature	Value
Cores	8
Core width	8
Frequency	5GHz
Private L1 I\$	32KB
Private L1 D\$	512KB
Shared L2	8MB

High cache miss rates indicate low locality in Google **Workload Traces compared to** traditional HPC benchmarks.





**GAP Benchmark Suite** 



### References

#### [1] https://dynamorio.org/google\_workload\_traces.html. [2] Ayers et al., "Asmdb: understanding and mitigating front-end stalls in warehouse-scale computers" in ISCA 2019.